SESSION 16 – TAPA I
Advanced Transistor Technology III

Thursday, June 17, 8:00 a.m.
Chairpersons: S. Deleonibus, LETI
C.H. Diaz, TSMC

16.1 — 8:00 a.m.
On the Integration of CMOS with Hybrid Crystal Orientations, M. Yang, V. Chan*, S.H. Ku*, M. Ieong, L. Shi, K.K. Chan, C.S. Murthy*, R.T. Mo*, H.S. Yang*, E.A. Lehner*, Y. Surpris*, F.F. Jamin*, P. Oldiges*, Y. Zhang, B.N. To, J.R. Holt*, S.E. Steen, M.P. Chudzik*, D.M. Fried*, K. Bernstein, H. Zhu*, C. Y. Sung*, J. A. Ott, D.C. Boyd* and N. Rovedo*, IBM SRDC, Yorktown Heights, NY, *IBM, Hopewell Junction, NY

Hybrid orientation technology using pFETs on (110) surface orientation and nFETs on (100) orientation is promising for future CMOS applications. However there are many issues on device design and process integration regarding the new structure and (110) surface orientation, such as device isolation, epitaxy quality and scalability, dopant implantation, and the mixture of SOI and bulk devices. These issues are addressed in detail in the present work. Ring oscillators using HOT CMOS have been demonstrated for the first time, with Lpoly about 85nm and tox=2.2nm, resulting in 21% improvement from (100) control.

16.2 — 8:25 a.m.
An Enhanced 90nm High Performance Technology with Strong Performance Improvements from Stress and Mobility Increase through Simple Process Changes, R. Khamankar, H. Bu, C. Bowen, S. Chakravarthi, P.R. Chidambaram, M. Bevan, A. Krishnan, H. Niimi, B. Smith, J. Blatchford, B. Hornung, J.P. Lu, P. Nicollian, B. Kirkpatrick, D. Miles, M. Hewson, D. Farber, L. Hall, H. AlShareef, A. Varghese, A. Gurba, V. Ukraintsev, B. Rathsack, J. DeLoach, J. Tran, C. Kaneshige, M. Somervell, S. Aur, C. Machala and T. Grider, Texas Instruments, Dallas, TX

In this abstract we present a highly manufacturable, high performance 90nm technology with best in class performance for 35nm gate-length N and P transistors. Unique, but simple and low cost, process changes have been utilized to modulate channel stress and implant profile to generate enhanced performance with no additional masks. High drive currents of 1193uA/um and 587uA/um are obtained for nMOS and pMOS transistors respectively at 1.2V Vdd and an Ioff of 60nA/µm. An industry leading 90nm technology CV/I of 0.61ps and1.12ps are obtained for nMOS and pMOS transistors respectively. An aggressively scaled 12Å EOT plasma-nitrided, cluster gate dielectric is used. Process conditions are optimized to obtain high drive current, good Vt roll-off control and simultaneously meet reliability requirements.

16.3 — 8:50 a.m.
New Guideline of Vdd and Vth Scaling for 65nm Technology and Beyond, E.Morifuji, T.Yoshida, H.Tsuno, Y.Kikuchi, S.Matsuda, S.Yamada, T.Noguchi and M.Kakumu, Toshiba Corporation, Yokohama, Japan

We show new guideline of Vdd and Vth scaling for logic blocks and high density SRAM cell from low power viewpoint. New degradation mode for inverter delay becomes major obstacle for Vdd scaling in the future. Low Vdd and low Vth should be applied only for circuits with high switching activity. In other portions, Vdd should be kept around 1-1.2V. High density SRAM(0.56um2) with beta ratio of 1 operates at 0.7V by choosing optimum Vth.

16.4 — 9.15 a.m.
High Performance CMOSFET Technology for 45nm generation, A. Oishi, T. Komoda, Y. Morimasa, T. Sanuki, H. Yamasaki, M. Hamaguchi, K. Oouchi, K. Matsuo, T. Iinuma, T. Itoh, Y.Takegawa, M. Iwai, K. Sunouchi and T. Noguchi, Toshiba Corporation, Yokohama, Japan

High performance CMOSFET process design for 45nm generation is demonstrated. Activation policy is shown to achieve high performance source and drain extension, high gate activation and defect-less source and drain (SD) simultaneously. Serious problem of phosphorus TED is investigated and suppressed by appropriate activation process designing. Good Vth roll-off and Ion-Ioff characteristics are achieved for 20nm gate MOSFET by utilizing ultrahigh speed annealing, disposable sidewall spacer, phosphorus n+ SD and appropriate activation process designing.

16.5 — 9:40 a.m.
Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique, A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida and J. Koga, Toshiba Corporation, Yokohama, Japan

A novel approach for achieving high-performance Schottky-source/drain MOSFETs(SBTs: Schottky Barrier Transistors) is proposed. The dopant segregation (DS) technique is employed and significant modulation of Schottky barrier height is demonstrated. The DS-SBT fabricated with the current CoSi2 process show competitive drive current and better short-channel-effect immunity, compared to the conventional MOSFET. In conclusion, the DS-Schottky junction is useful for the source/drain of advanced MOSFETs.